

Optimization Opportunities and Pitfalls when Implementing High Performance 2D Convolutions

S4297

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ł	Filter			Ima	age		Output			
3	3	1	1	2	3	1				
1	1	2	4	5	2	3				
1	2	3	4	1	1	5				
			1	2	5	2				

For all image pixels For all filter elements output += In(x,y)*Fil(x,y)



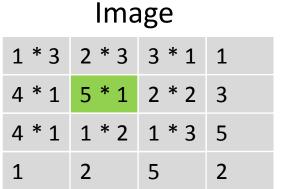
Filte	er		Im	age		Output			
3	3 1	1	2	3	1				
1	1 2	4	5	2	3				
1	2 3	4	1	1	5				
		1	2	5	2				

For all image pixels For all filter elements output += In(x,y)*Fil(x,y)

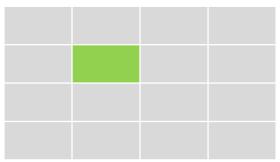


	Filter		
3	3	1	1 * 3
1	1	2	4 * 1
1	2	3	4 * 1

_ . .







For all image pixels
 For all filter elements
 output += In(x,y)*Fil(x,y)

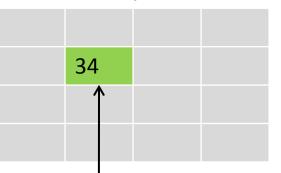


	Filter		
3	3	1	1 * 3
1	1	2	4 * 1
1	2	3	4 * 1

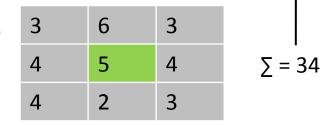
Intage										
1 * 3	2 * 3	3 * 1	1							
4 * 1	5 * 1	2 * 2	3							
4 * 1	1 * 2	1 * 3	5							
1	2	5	2							

Imaga

Output



For all image pixels
 For all filter elements
 output += In(x,y)*Fil(x,y)



2D Convolutions



Tesla K20 GFLOPS = 3521 GFLOPS BW 208 GB/s = 52 GigaFLOAT/s → 3521 GFLOPS/ 52 GFLOAT/s = 67 FLOPS / FLOAT is the theoretical break-even between bandwidth bound and compute bound.

The number of computations per output element in a 2D convolution is filter size * filter size * 2. \rightarrow filter size = $\sqrt{2 * 67}$ = 11.5 \rightarrow break-even between compute and bandwidth bound. *A 13*13 2D convolution is in theory compute bound for the Tesla K20.* Smaller sizes are bandwidth bound.

The Tesla K20

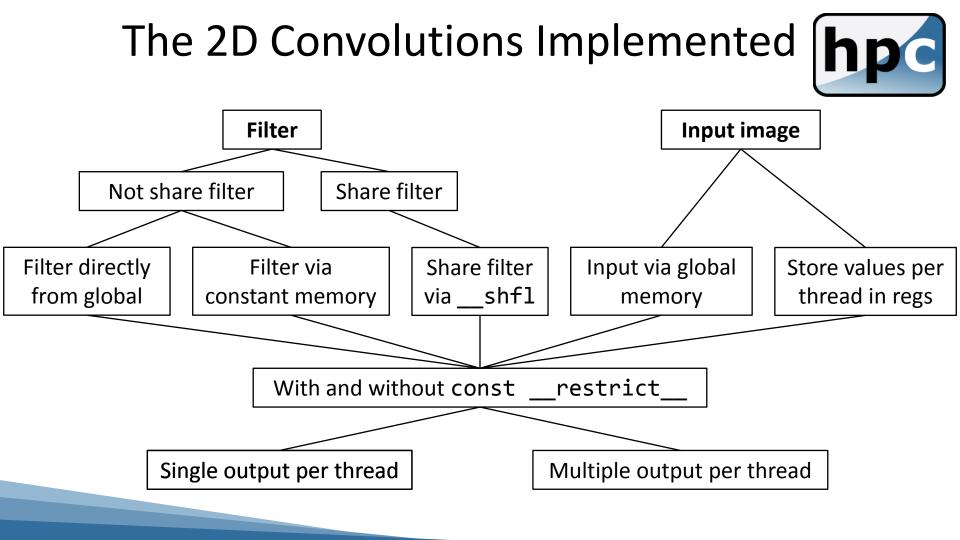
Kepler 110 Whitepaper

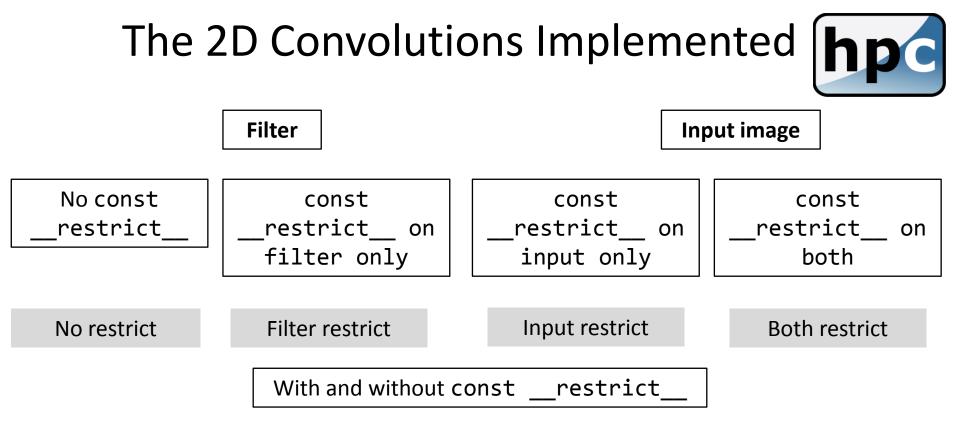
"192 single-precision floating point units""32 load/store units (LD/ST)"

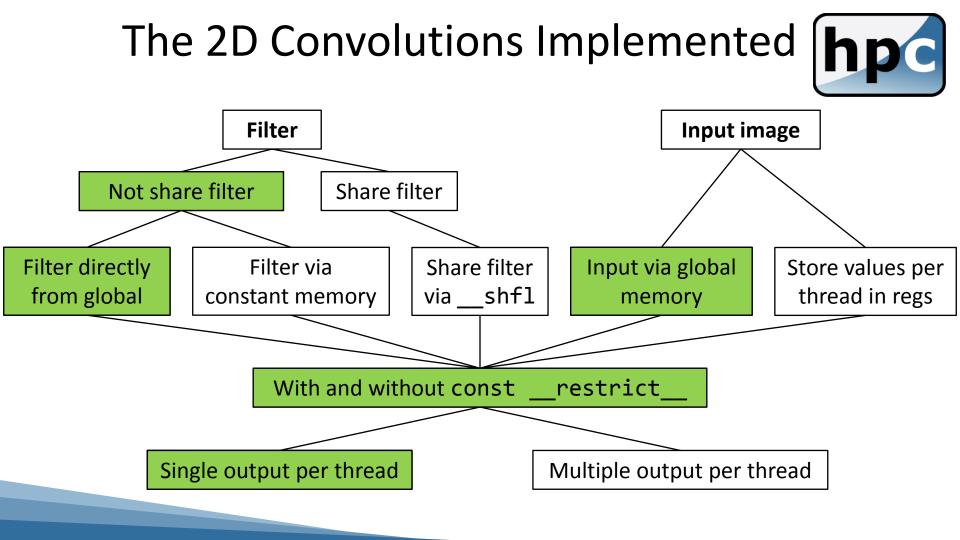
→ 6 FMADs per LD/ST

2.0 Viewport Transform Stream Output
Stream Output
arp Scheduler Warp Scheduler
h Unit Dispatch Unit Dispatch Unit Use and Unit
* * * * * * * *
Core Core Core Core LDIST SFU
Core Core Core Core LDIST SFU
Core Core Core Core LDIST SFU
Core Core Core Core LD/ST SFU
Core Core Core Core LD/ST SFU
Core Core Core Core LD/ST SFU
╺─┼╾┼╾┼╾┼═╣─╴
Core Core Core Core LD/ST SFU
Core Core Core Core LDIST SFU
Core Core Core Core LD/ST SFU
Core Core Core Core LD/ST SFU
Core Core Core Core LD/ST SFU
Core Core Core Core LDIST SFU
Core Core Core Core LD/ST SFU
Core Core Core Core LD/ST SFU
Core Core Core Core LDIST SFU
Core Core Core Core LDIST SFU
L1 Cache







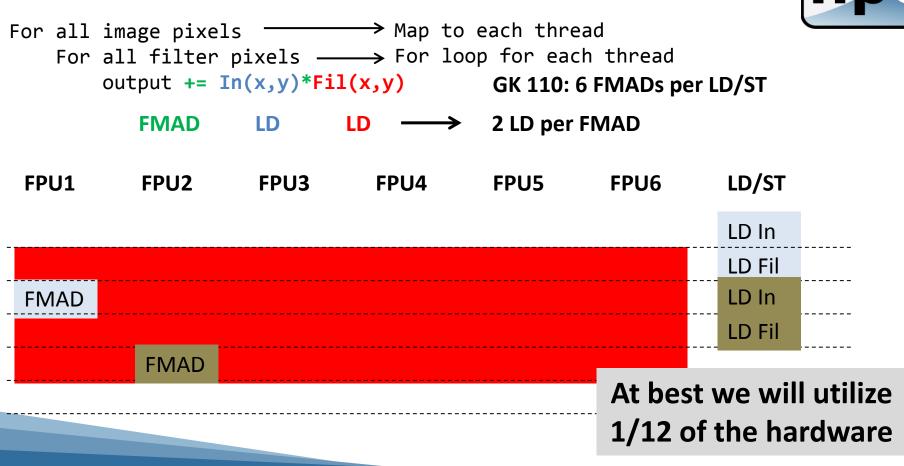


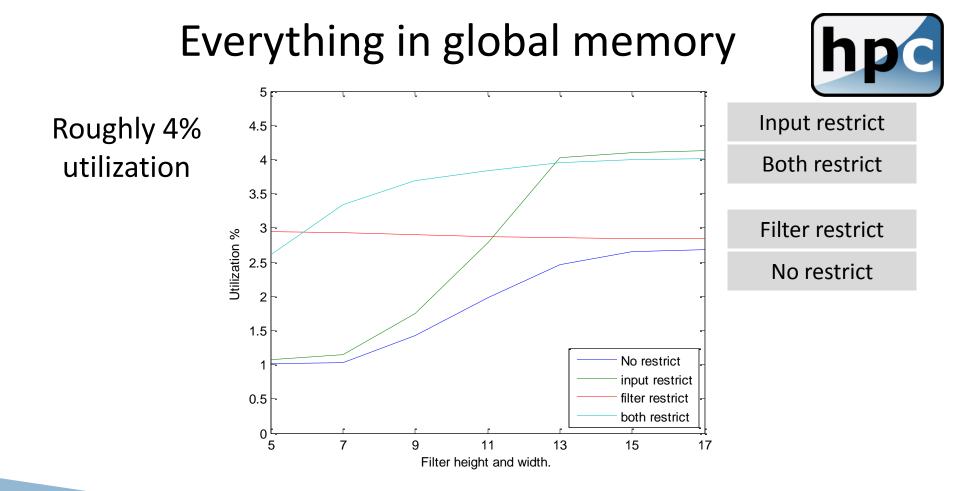
Everything in global memory

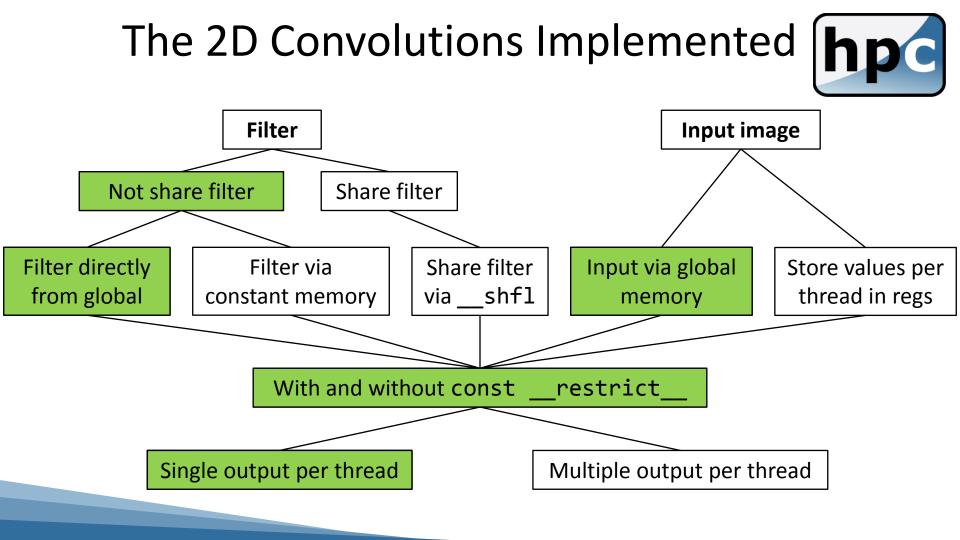
For all image pixels → Map to each thread
For all filter pixels → For loop for each thread
output += In(x,y)*Fil(x,y)

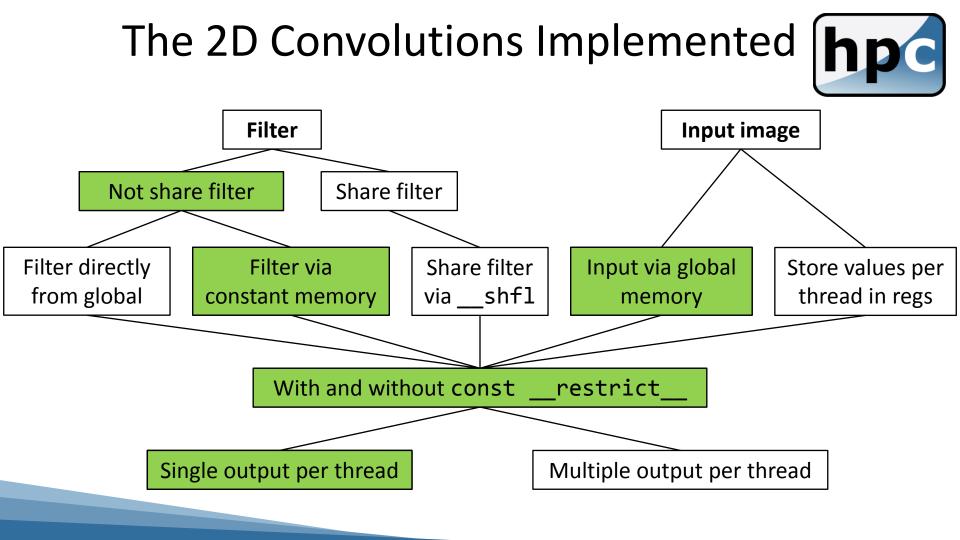


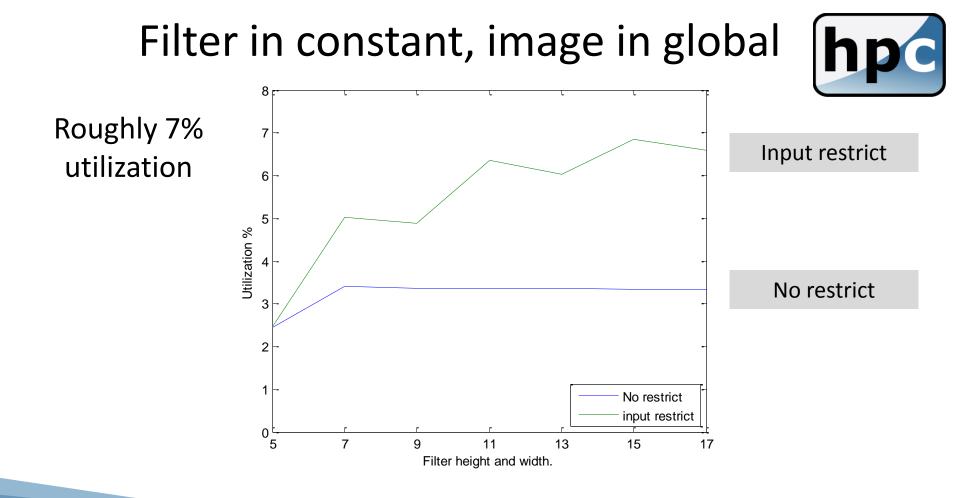
Everything in global memory

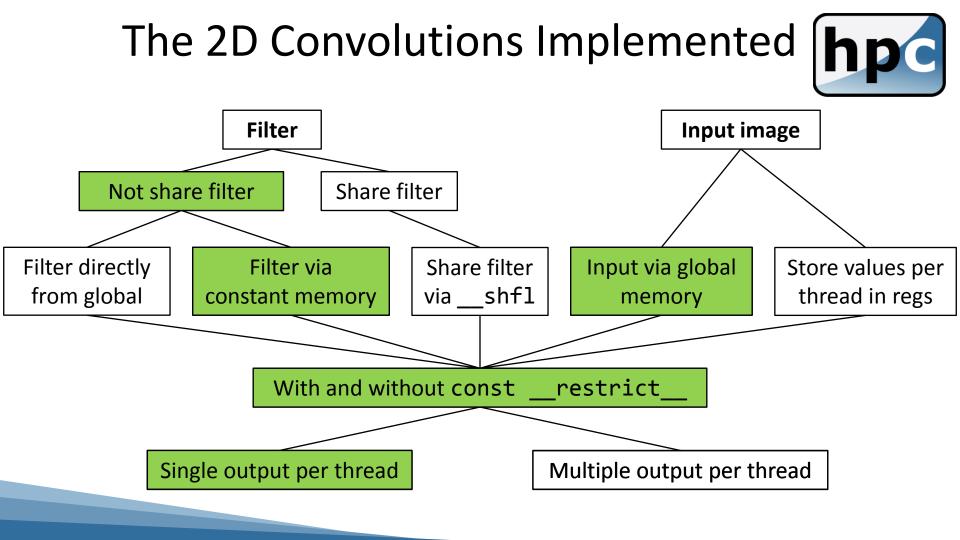


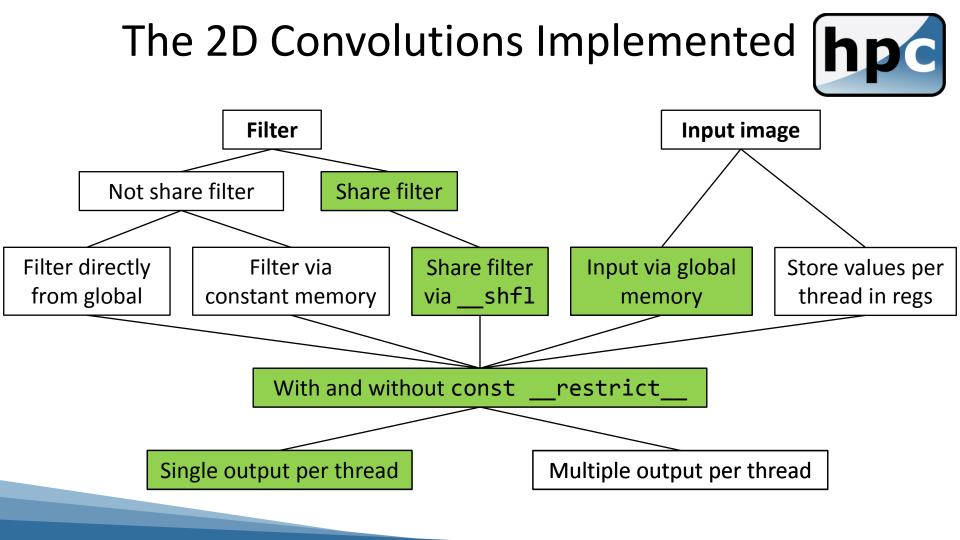


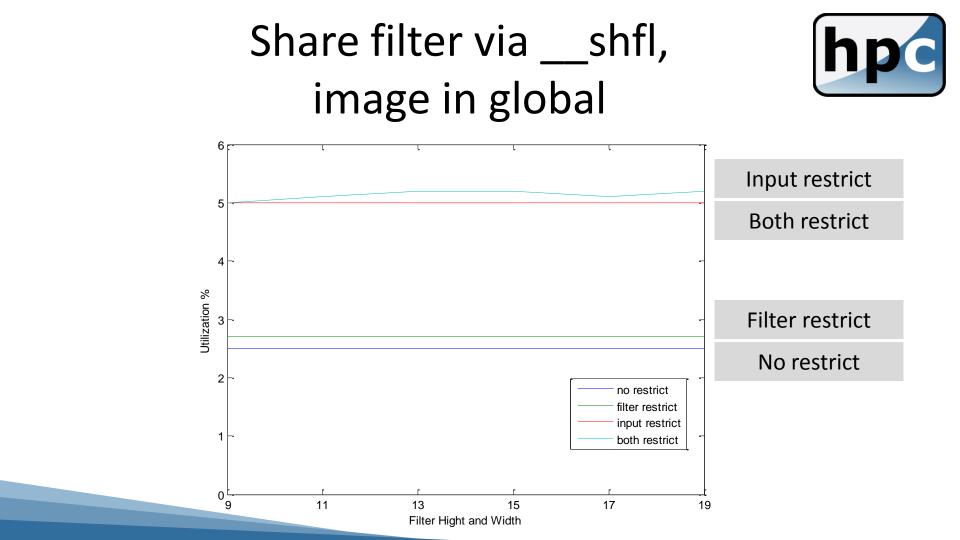


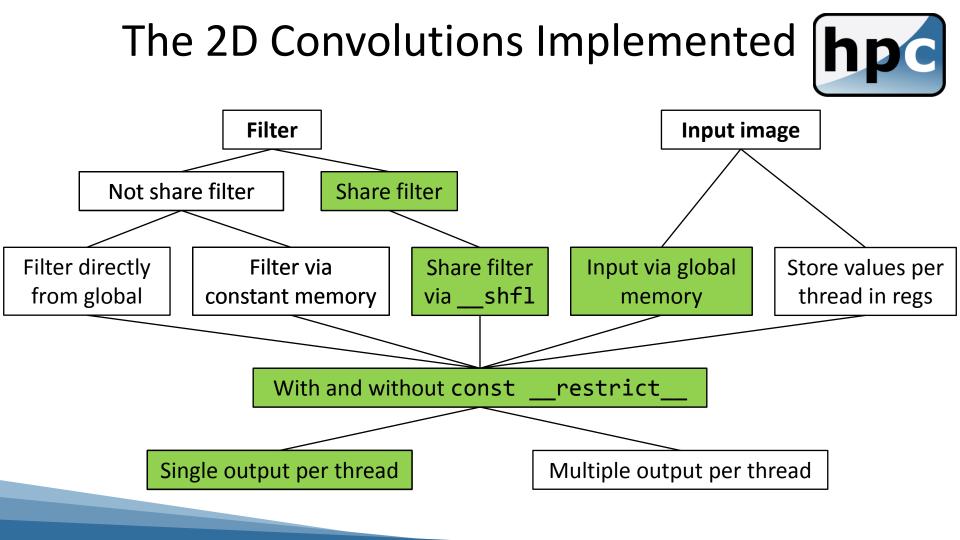


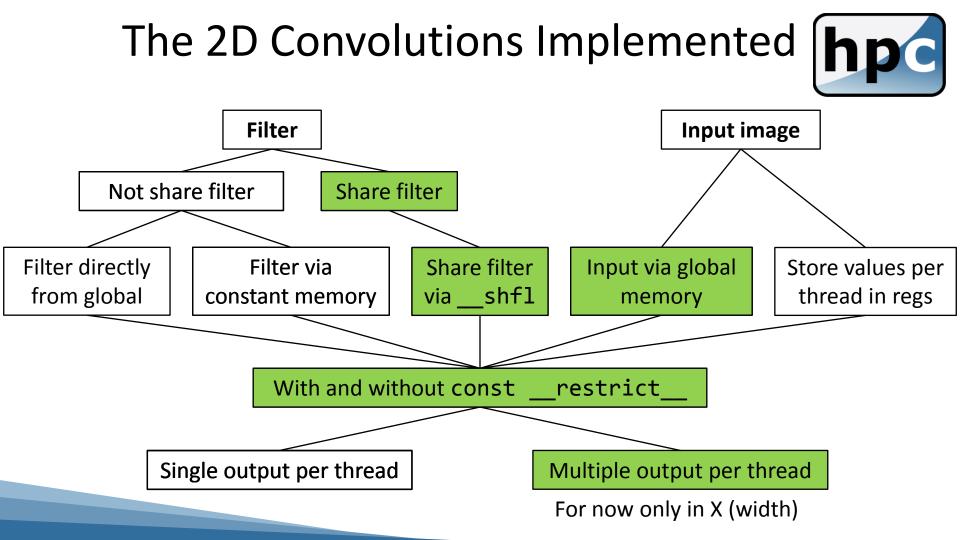


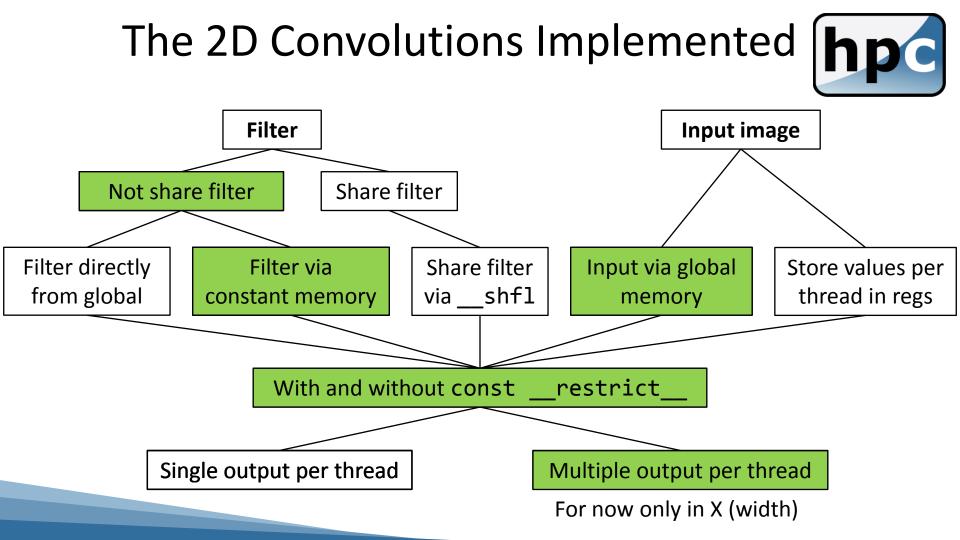










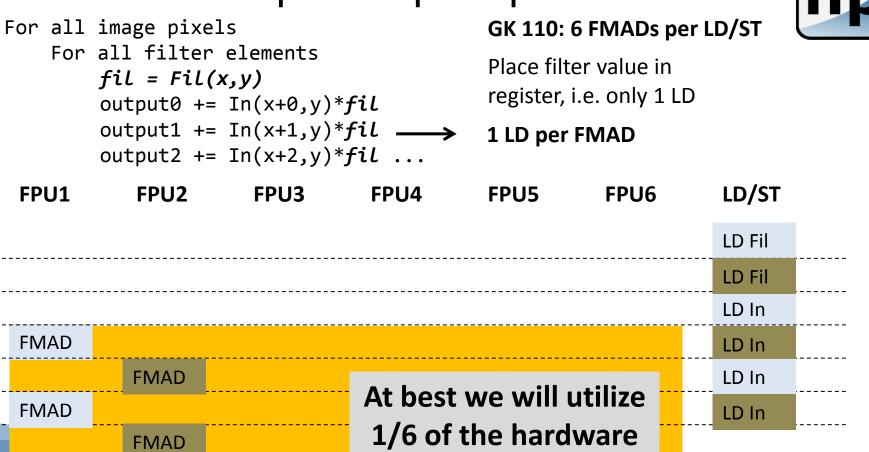


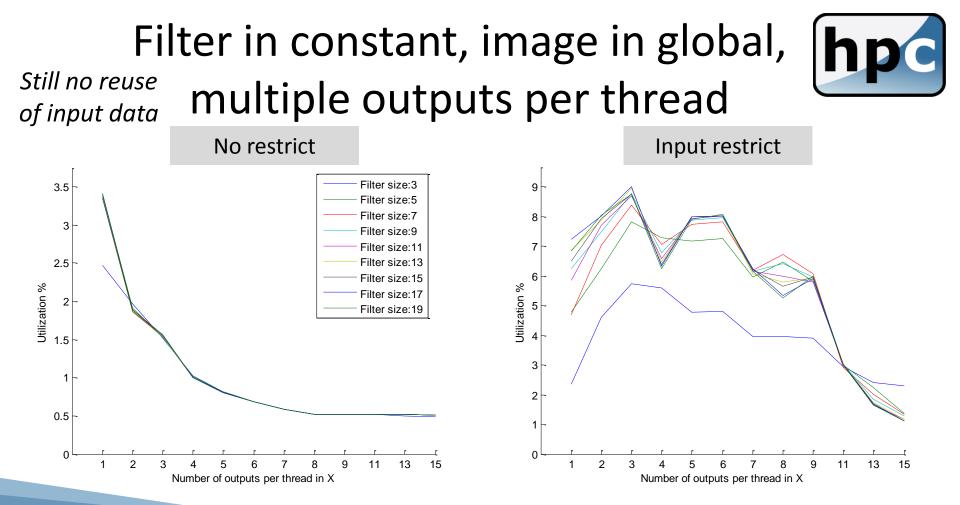
Multiple outputs per thread

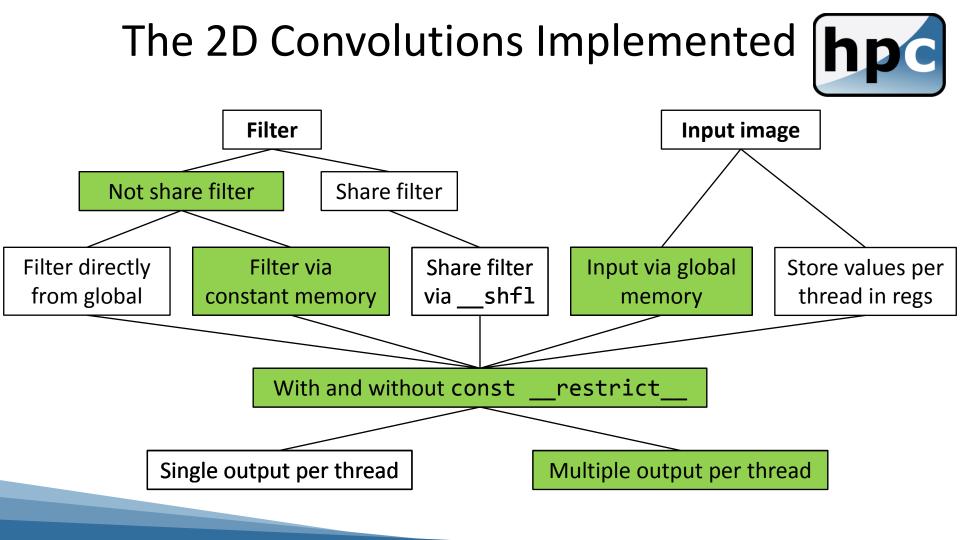


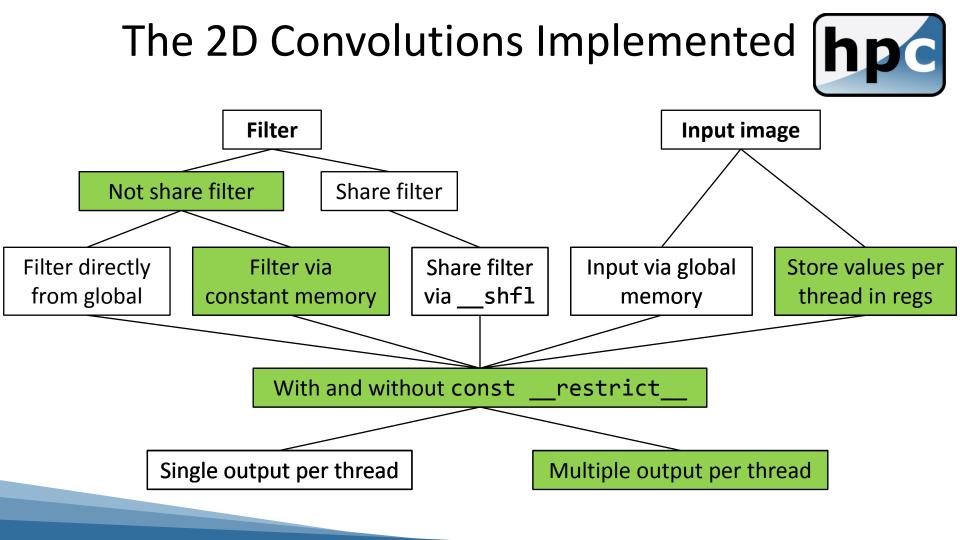
For all image pixels → Map to each thread
For all filter elements → For loop for each thread
output += In(x.y)*Fil(x,y)

Multiple outputs per thread









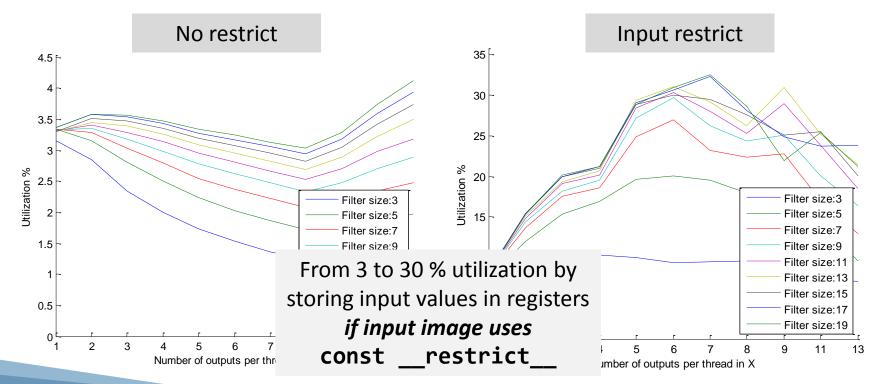
For	<pre>image pixels all filter elements fil0 = Fil(x+0,y); in0 = In(x+0,y); in1 = In(x+1,y) output0 += in0*fil0</pre>	Load filter into register. Load all input elements into register.	h
		into register.	
	output1 += in1* <i>fil0</i> output2 += in2* <i>fil0</i>	Do all FMAs.	

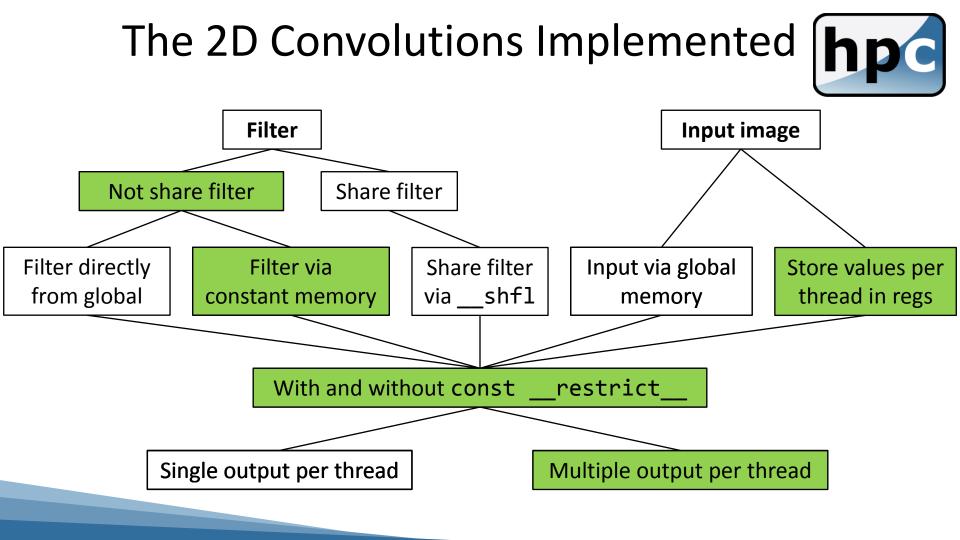
p

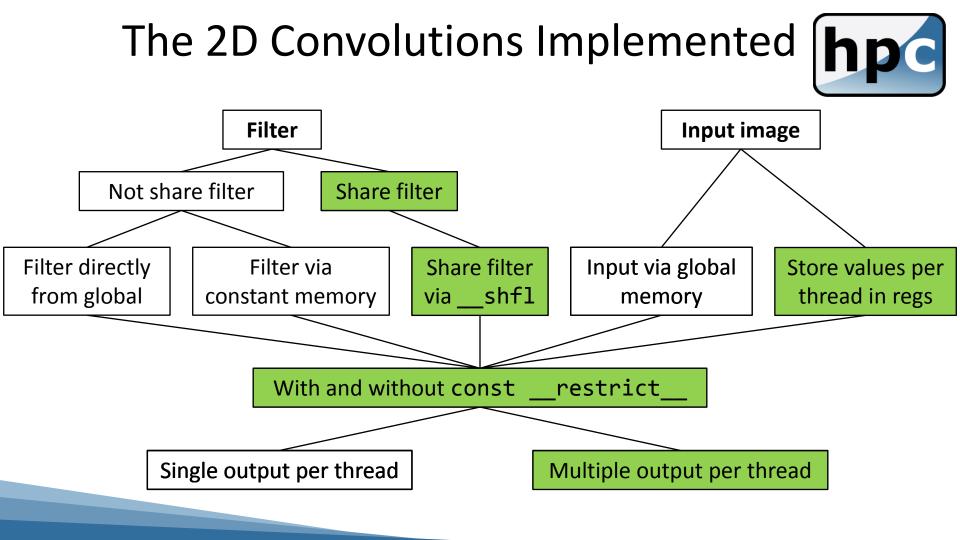
FPU1	I	FPU2 F		FPU3	PU3 FPU4 FPU5		FPU6	LD/ST
	Filter-size*2						 LD filter	
	operations per load							 LD all In
FMAD				UL UL		perioau		 LD filter
FMAD								LD all In
FMAD		FMAD						 LD filter
FMAD		FMAD						 LD all In
FMAD		FMAD		FMAD				

Filter via const, reusing thread local input, multiple outputs per thread



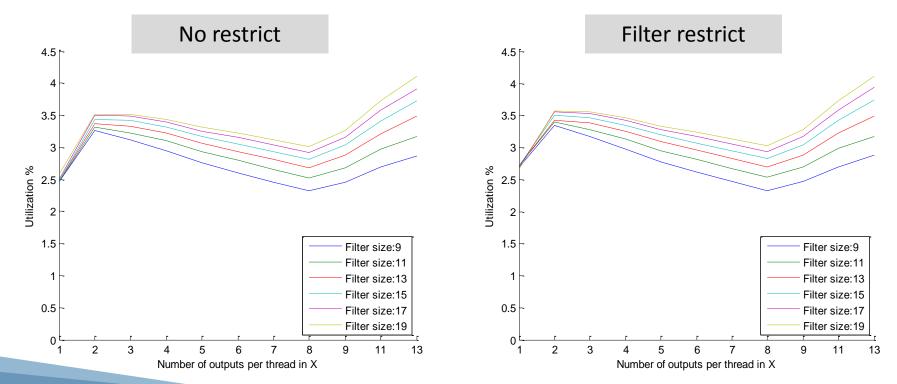






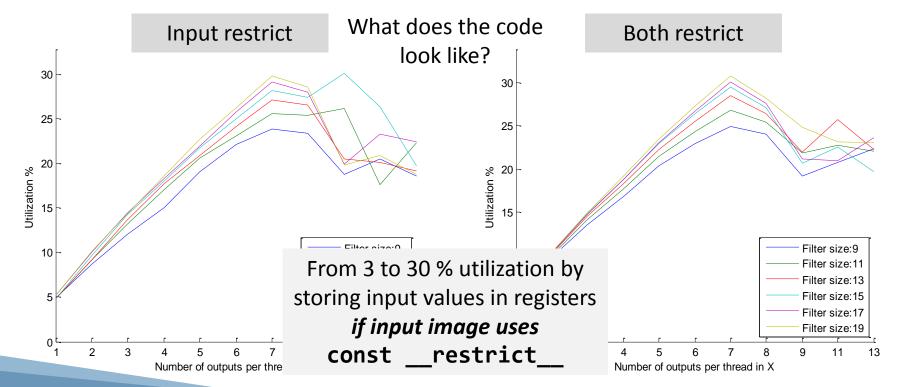
Sharing filter via shfl, reusing thread local input, multiple outputs per thread





Sharing filter via shfl, reusing thread local input, multiple outputs per thread





For	<pre>image pixels all filter elements fil0 = Fil(x+0,y); in0 = In(x+0,y); in1 = In(x+1,y) output0 += in0*fil0 output1 += in1*fil0 output2 += in2*fil0</pre>	Load filter into register. Load all input elements into register. Do all FMAs.	h
	output2 += in2* <i>fil0</i>	DO AII FIVIAS.	

p

FPU1	FPU2 FI		FPU3	PU3 FPU4 FPU5		FPU6		LD/ST		
	Filter-size*2							LD filter		
	operations per load								LD all In	
FMAD				OF	Jerations	perioau			LD filter	
FMAD									LD all In	
FMAD		FMAD							LD filter	
FMAD		FMAD							LD all In	
FMAD		FMAD		FMAD						

4 lines of code for reading input into register
9 lines of code for filter loop (shown below)
9 lines of code for output clean-up
= 22 lines of code. → Maintainable

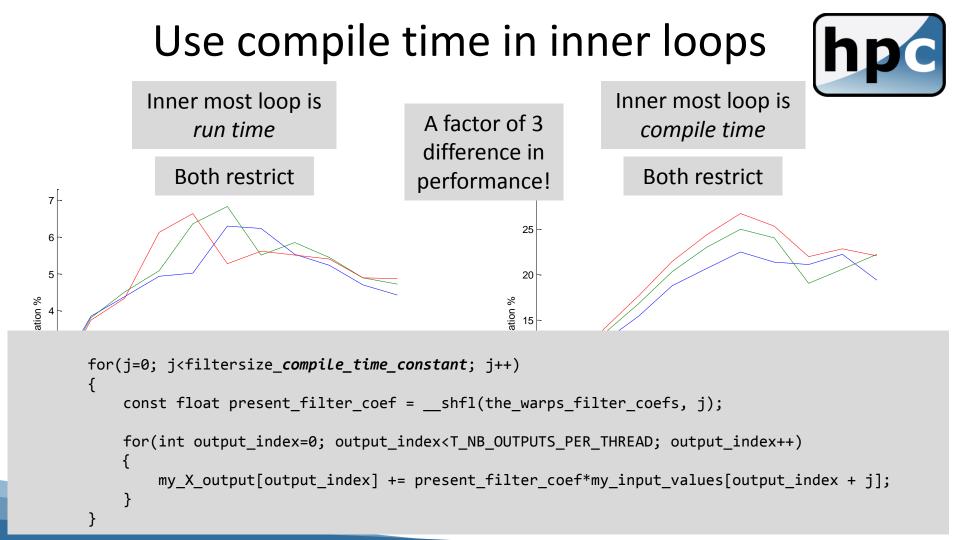
121	<pre>for(i=0; i<t_filter_width; (<="" i++)="" pre=""></t_filter_width;></pre>	1533312	
122	<pre>if(threadIdx.x < T_FILTER_WIDTH) {</pre>	766656	
123	<pre>the_warps_filter_coefs = filter_coefs[threadIdx.x + i*T_FILTER_WIDTH];</pre>	1916640	
124	3		
125			
126	<pre>const int input_data_float_offset = line_width * y_input_pos + x_block_pos + (i - half_filter_width) * line_width</pre>		
127			
128	load_data_float <nb_float_input_values>(my_input_values, input_data, input_data_float_offset);</nb_float_input_values>		
129			
130	<pre>for(j=0; j<t_filter_width; j++)="" pre="" {<=""></t_filter_width;></pre>		
131	// Shuffle to get the filter value from thread j;		
132	<pre>present_filter_coef =shfl(the_warps_filter_coefs, j);</pre>		
133			
134	<pre>for(int output_index=0; output_index<t_nb_outputs_per_thread; output_index++)="" pre="" {<=""></t_nb_outputs_per_thread;></pre>		
135	<pre>my_X_output[output_index] += present_filter_coef*my_input_values[output_index + j];</pre>	44466048	1
136	}		
137	3		
138	}		

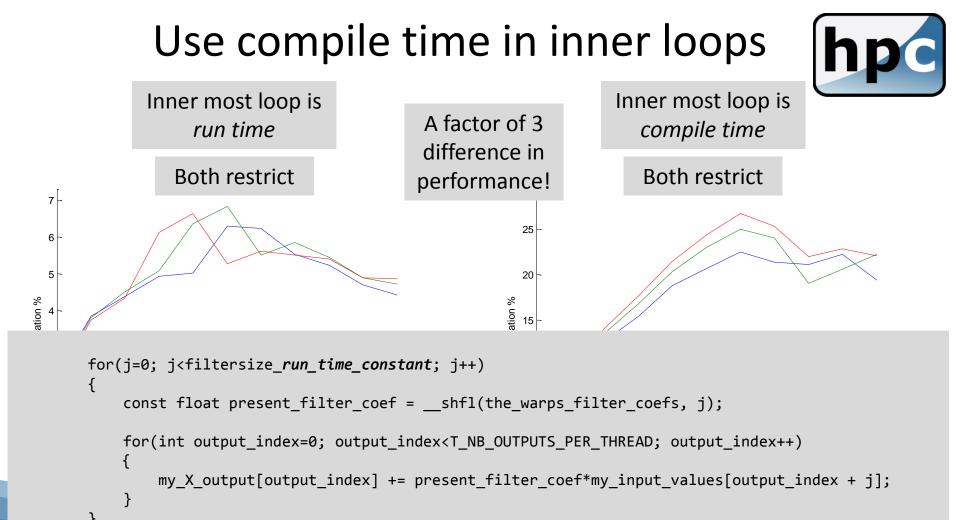
No hand-coded assembly No explicit use of textures No use of constant memory

Instead:

C++ Templates, const __restrict__, __shfl

-														_
				Instruct	Thread	Threa	Branche	Branc	Memory Type	Mem	Memor		L2	^
	Line	Address	Source	Execute	Instruction Executed	Execu Efficie	Taken	Efficie	Memory Type	Acces Type	Access	Id III	Tri Ov	
	179	11D3A0	FFMA.FTZ R34, R35, R12, R34;		12266496							Tr		
		11D3A8	FFMA.FTZ R35, R33, R11, R20;		12266496									
		11D3B0	FFMA.FTZ R19, R33, R15, R30;		12266496									
٦		11D3B8	FFMA.FTZ R39, R41, R12, R35;		12266496									1.
٠I		11D3C8	FFMA.FTZ R18, R33, R7, R18;		12266496									
		11D3D0	FFMA.FTZ R37, R41, R10, R19;		12266496									
		11D3D8	FFMA.FTZ R22, R33, R10, R22;		12266496									
		11D3E0	FFMA.FTZ R21, R33, R8, R21;		12266496									
		11D3E8	FFMA.FTZ R32, R33, R12, R32;		12266496									
		11D3E0	FFMA.FTZ R21, R41, R11, R21;		12266496	-								
		11D3F0	FFMA.FTZ R20, R33, R14, R34;		12266496									
		11D3F8	FFMA.FTZ R34, R41, R9, R36;		12266496									
		11D410	FFMA.FTZ R36, R41, R6, R31;		12266496									
		11D418	FFMA.FTZ R31, R41, R15, R18;		12266496			••	400					
		11D420	FFMA.FTZ R18, R41, R8, R22;		12266496				100	H	IVI.	ΑI		
		11D428	FFMA.FTZ R4, R41, R7, R4;		12266496					•				
		11D430	FFMA.FTZ R22, R41, R14, R32;		12266496							_		
	196	11D438	TEXDEPBAR 0x3;	383328	12266496	100.0								
		11D448	FFMA.FTZ R30, R33, R16, R38;	383328	12266496	100.0								
	198	11D450	SHFL.IDX PT, R33, R0, 0x7, 0x1f;	383328	12266496	100.0								
	199	11D458	FFMA.FTZ R20, R41, R16, R20;	383328	12266496	100.0								
	200	11D460	FFMA.FTZ R6, R33, R6, R34;	383328	12266496	100.0								
	201	11D468	FFMA.FTZ R34, R33, R7, R36;	383328	12266496	100.0								
	202	11D470	FFMA.FTZ R36, R33, R10, R31;	383328	12266496	100.0								
	203	11D478	FFMA.FTZ R31, R33, R11, R18;	383328	12266496	100.0								
	204	11D488	FFMA.FTZ R32, R33, R8, R37;	383328	12266496	100.0								
	205	11D40	FFMA.FTZ R37, R33, R14, R39;	383328	12266496	100.0								
	206	11D-98	FFMA.FTZ R32, R3, R11, R32;	383328	12266496	100.0								
	207	1104A0	TEXDEPBAR 0x2;	383328	12266496	100.0								
	208	1D4A8	FMA.FTZ R30, R41, R13, R30;	383328	12266496	100.0								_
	209	11D480	FFMA.FTZ R21, R33, R12, R21;	383328	12266496	100.0								-
	210	11D4B8	FFMA.FTZ R22, R33, R16, R22;	383328	12266496	100.0								
	1	11D4C8	FFMA.FTZ R38, R33, R15, R4;	383328	12266496	100.0								
	12	11D4D0	MOV R4, RZ;	383328	12266496	100.0								
		11D4D8	FFMA.FTZ R40, R33, R13, R20;		12266496									
1		11D4E0	FFMA.FTZ R20, R3, R12, R31;		12266496									
		11D4E8	FFMA.FTZ R18, R3, R15, R34;		12266496									
		11D4F0	FFMA.FTZ R19, R3, R16, R37;		12266496									
		11D4F8	FFMA.FTZ R31, R3, R14, R21;		12266496									
		11D508	TEXDEPBAR 0x1;		12266496									
		11D510	FFMA.FTZ R39, R33, R5, R30;		12266496									
		11D518	FFMA.FTZ R16, R3, R13, R22;		12266496									
		11D518	FFMA.FTZ R30, R3, R7, R6;		12266496									
		11D520	FFMA.FTZ R34, R3, R10, R38;		12266496									
			FFMA.FTZ R33, R3, R8, R36;											
		11D530			12266496									
		11D538	FFMA.FTZ R22, R3, R5, R40;		12266496									
		11D548	TEXDEPBAR 0x0;		12266496									
	226	11D550	FFMA.FTZ R21, R3, R2, R39;		12266496									Ŧ





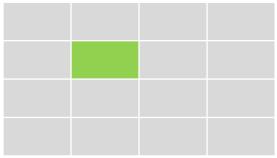


F	ilter		
3	3	1	1 *
1	1	2	4 *
1	2	3	4 *

--1.

Image					
1 * 3	2 * 3	3 * 1	1		
4 * 1	5 * 1	2 * 2	3		
4 * 1	1 * 2	1 * 3	5		
1	2	5	2		

Output



2D Convolutions

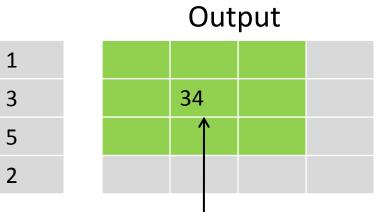
5

2

1



Filter			Image		age
3	3	1	1 * 3	2 * 3	3 * 1
1	1	2	4 * 1	5 * 1	2 * 2
1	2	3	4 * 1	1 * 2	1 * 3



Extend reuse of input data to Y also.

3	6	3	
4	5	4	
4	2	3	

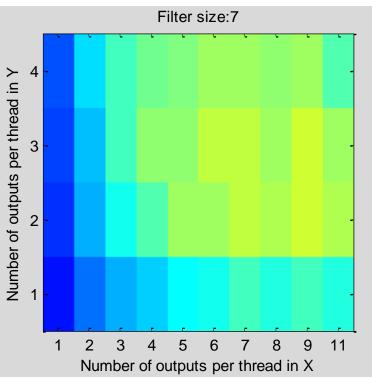
Reuse input in X and Y



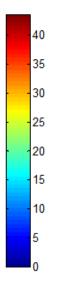
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Reuse input in X and Y

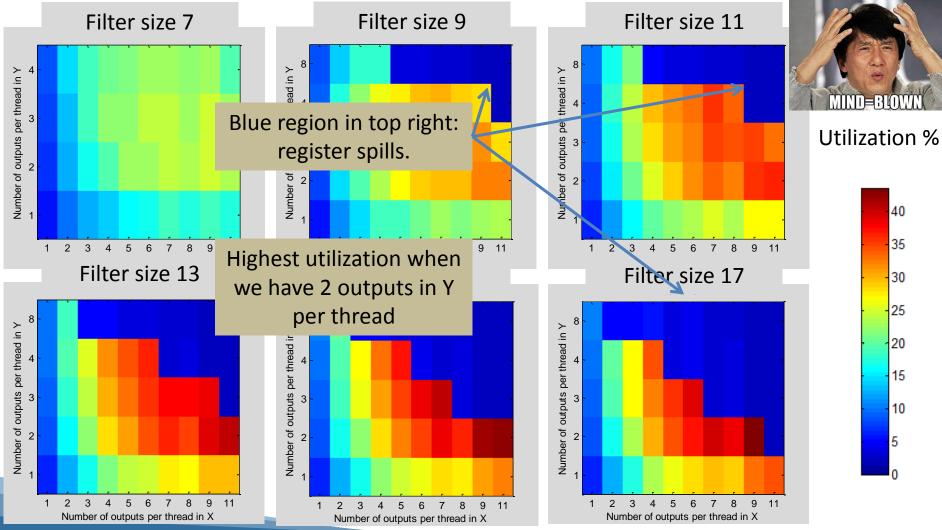
Multiple outputs per thread in Y (height)



Utilization heat map: blue is low utilization, red is high utilization.



Multiple outputs per thread in X (width)



2D Convolutions Conclusion



DOs:

- Map multiple outputs to each thread.
- Use templates to hardcode loops as non-constant indexed arrays "[are] likely to [be] placed in local memory".
- Its helpfull to have a basic understanding and model of the hardware you're working with.
- Keep looking at you assembly: What lines map to register based compute, and what is LD/ST integer spaghetti code?

DON'Ts:

- Use run-time sizes in inner most loops.
- Use textures or constant memory. const ____restrict___gets the job done and its very simple to use!

Any questions?

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